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FPGA Based Low Power Digital Frequency Synthsizer

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ABSTRACT: We use a digital frequency synthesizer in our system to generate a sampled sinusoidal wave of frequency 1 MHz (can be change based on user requirement) estimated carrier frequency offset. The major advantage of Digital Frequency Synthesizer (DFS) is that its output frequency, phase and amplitude can be precisely and rapidly manipulated under the control of a DSP. Other inherent DFS attributes include the ability to tune with extremely fine frequency and phase resolution and to rapidly "hop" between the frequencies. Important advantage of implemented design is we can hop any frequencies based on user requirement only by changing binary word called as frequency controlled word.

Keywords: DFS, CORDIC, Phase Accumulator, DSP.

I. INTRODUCTION

Various techniques are available in the literature for quarter wave memory compression, such as Sine-phase difference algorithm, Taylor series expansion, Modified Sunderland Architecture, Nicholas' Architecture, CORDIC (CO-ordinate Rotation Digital Computer) Algorithm. The implicit goal of these phase-to-sine conversion techniques is to reduce the maximum amplitude error for any phase angle, in effect mimicking the behavior of a LUT.

In pursuing this goal, all architectures become complex in one way or the other. Also, the ROM size becomes fairly large as it grows exponentially with the width of the phase accumulator whereas a large phase accumulator width is desirable in order to achieve fine frequency tuning. Truncating the phase accumulator output, on the other hand, introduces spurious harmonics. We use a digital frequency synthesizer in our system to generate a sampled sinusoidal wave of frequency 1 MHz and 2 MHz The major

Advantage of Digital Frequency Synthesizer (DFS) is that its output frequency, phase and amplitude can be precisely and rapidly manipulated under the control of a DSP. Other inherent DFS attributes include the ability to tune with extremely fine frequency and phase resolution and to rapidly "hop" between the frequencies. These combined characteristics have made this technology popular in military, radar and communication systems. The digital circuits used to implement signal processing functions do not suffer the effects of thermal drifts, aging and component variations associated with their analog counterparts. The implementation of digital functional blocks makes it possible to achieve a high degree of system integration. Recent advances in IC fabrication technology, particularly the CMOS technology coupled with advanced DSP algorithms and architectures provide possible single chip solutions to complex communication and signal processing sub-systems such as modulators, demodulators, local oscillators, programmable clock generators, cellular base stations and wireless local loop base stations.

The paper is organized as follows. In Section 2, the DFS Description is briefly presented. In Section 3, DFS Architecture given with details. In Section 4Experimental results and Discussions is explored. In Section 5 The verification of the implemented digital modulators through simulations and real-time results acquired from the implementation into the FPGA SPARTN 3 board are emphasized and evaluated finally, in Section 6, conclusions are drawn.

II. DFS DESCRIPTION

The DFS is shown in a simplified form in Fig. 1. It consists of a phase accumulator and a phase to amplitude converter (conventionally a sine ROM). The phase accumulator consists of a j bit frequency register, which stores a digital phase increment word followed by a j bit full adder and a phase register. The digital input phase increment word is entered in the frequency register. At each clock pulse, this data is added to the data previously held in the phase register.

The phase increment word represents a phase angle step that is added to the previous value at each $(1/f_{clk})$ second to produce a linearly increasing phase value.

The phase is generated by modulo 2^j overflowing property of a phase accumulator. The rate of overflow is the output frequency, expressed as

$$f_{out} = \frac{\Delta P f_{clk}}{2^j} \qquad \forall\, f_{out} \le \frac{f_{clk}}{2}, \quad \ldots\ldots\ldots (1)$$

where ΔP is the phase increment word, j is the number of phase accumulator bits, f_{clk} is the clock frequency and f_{out} is the output frequency. The constraint in the above equation comes from the sampling theorem. As the phase increment word is an integer, the frequency resolution is found by setting ΔP =1, as

$$\Delta f = \frac{f_{clk}}{2^j} \qquad \ldots\ldots(2)$$

The read only memory (ROM) is a look-up table, which converts the digital phase information into the values of a sine wave.

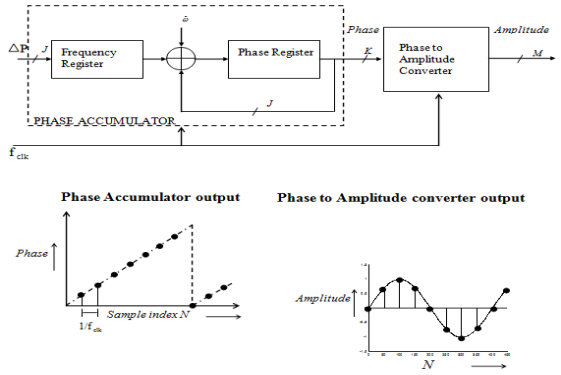

Fig.1. DFS Block diagram and wave forms.

According to the equations 1 and 2 we can able to calculate output frequency of modulated signal based on input FCW (frequency control word) value as shown table below.

A. Phase Accumulator

The phase accumulator comprises of a frequency register, an adder and a phase register as shown in Figure 1. The output of the phase register is fed back to the adder as one of its inputs. The other input of the adder comes from the frequency register. This second input, also called the frequency control word, is added to the previous phase sum on every clock cycle. A clock with frequency f_{clk} is the synthesizer's only time reference. The phase accumulator's output is thus a ramp, as it overflows to 0 periodically. Assuming an N-bit accumulator, the frequency of the ramp is given by

$$f_{out} = f_{clk} \times \frac{frequency\ control\ word}{2^N} \ldots\ldots(3)\ .$$

Every value at the output of the phase accumulator is converted to approximated sine amplitude by a phase-to-sine amplitude converter.

B. Phase to amplitude converter

The spectral purity of the DFS is also determined by the values stored in the sine table ROM. Therefore, it is desirable to increase the resolution of the ROM. Unfortunately, a larger ROM storage means higher power consumption, lower speed and greatly increased costs. The most elementary technique of compression is to store only $\pi/2$ radians of sine wave information and to generate the ROM samples for the full range of 2π by exploiting the quarter wave symmetry of the sine function. Methods of quarter wave symmetry include trigonometric identity, Nicholas' method and the Taylor series.

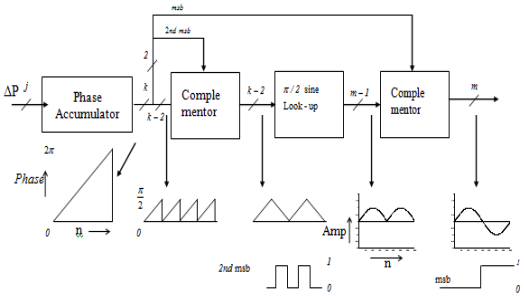

Fig. 2. Detailed diagrams of DFS.

First two msb bits (1st and 2nd bits) are used to complement the output of phase accumulator and output of sine look-up table respectively as shown in the figure 2 above.

III. DFS ARCHITECTURE

The phase to sine amplitude converter block includes a 1's complement to exploit quarter wave symmetry, as previously seen in other structures. Clearly, this architecture is significantly less complex than those of the other methods discussed previously.

It does not include a ROM. No multipliers or squaring circuits are required. Equal length segments are used to simplify the control circuitry. Only three integers need to be added and multiplexers shown in Figure.3 have been optimized by combining similar inputs and implemented in combinational logic.

The phase accumulator is 20 bits wide, truncated to 12 bits. The two MSBs are used for quadrant symmetry. The next three bits identify the segment. The remaining seven bits identify different sub-angles. The two upper multiplexers shift these remaining seven bits.

Architecture for digital frequency synthesizer is presented. The main advantage of this architecture is that it does not depend upon the extensive use of ROM, as is normally the case with other commonly available architectures. Hence, it fits into a very small area on the chip. Also, the spectral purity of its output is sufficient for the present system requirement.

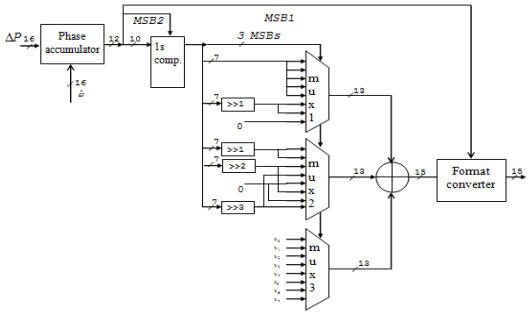

Fig. 3. DFS Architecture.

IV. EXPERIMENTAL RESULTS AND DISCUSSIONS

To verify the architecture, the design was coded in Verilog the design is simulated by using the simulator Modelsim SE6.3f. The simulated waveforms of different blocks are presented. The design is synthesized by using XILINX synthesize XST Tool from Xilinx ISE design suite 13.4 tool. The synthesis results and the result of each step are described.

A. Simulation Output

The design parameters used for the simulations were a 16-bit phase accumulator that generated 16-bit digital sine waves with frequencies of 1 MHzand 2MHz (the frequencies were arbitrarily selected). The simulation results for theDigital Frequency Synthesizer are shown in Figure 4below.

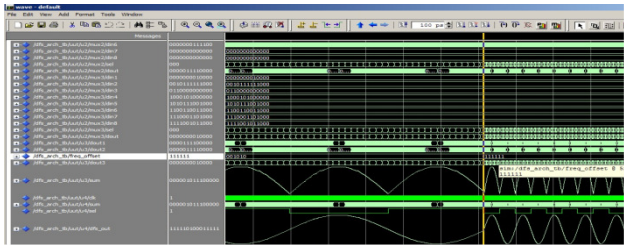

Fig. 4. Simulation output of DFS.

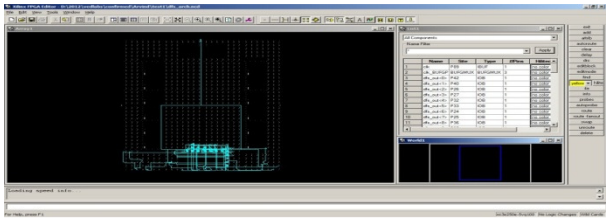

Fig. 5. Layout view of top module of DFS.

In this Digital Frequency Synthesizer uses 33,82,33,15 and 1 slice registers, slice LUTs, fully used LUT-FF pairs, bonded IOBs and BUFG/BUFCTRLs respectively as shown in figure 6 below

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	33	69120	0%
Number of Slice LUTs	82	69120	0%
Number of fully used LUT-FF pairs	33	82	40%
Number of bonded IOBs	15	640	2%
Number of BUFG/BUFGCTRLs	1	32	3%

Fig. 6. Design Summary of DFS.

B. Emulation Output

Emulation is nothing but verifying the synthesized result of design using hardware platform, Emulation result is observed on the chip scope pro logic analyzer by using Spartan 3 kit. Synthesized RTL code of DFS is ported into Spartan 3 Kit of Xilinx FPGA, finally we will capture emulation result of DFS generates 1MHz and 2 MHz sine waves on chip scope pro logic Analyzer software as shown in figure 7 below.

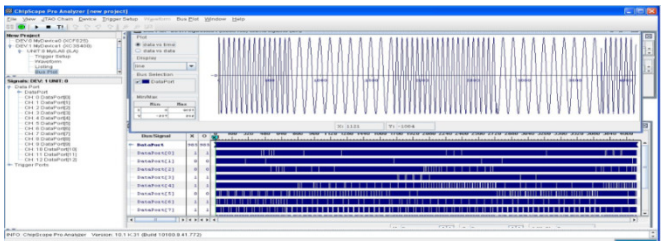

Fig. 7. Emulation result of BFSK

V. CONCLUSIONS

In this paper, we have presented a novel method exploiting the quadrant symmetry of trigonometric functions and trigonometric identities. A new Direct Digital Frequency Synthesizer architecture based on this technique was presented. We use a digital frequency synthesizer in our system to generate a sampled sinusoidal wave of frequency 1 MHz and 2MHz (can be change based on user requirement) estimated carrier frequency offset. This paper describes the design and implementation of a DFS on a FPGA platform. In future work, we will concentrate on transistor level simulation using CMOS technology.

REFERENCES

[1] J. Tierney, C. M. Rader and B. Gold, "A Digital Frequency Synthesizer," *IEEE Trans. Audio Electoracust*, vol.**19**, pp. 48–57, Mar.1971.

[2] L. K. Tan, E. W. Roth, G. E. Yee and H. Samueli, "An 800-MHz Quadrature Digital Synthesizer with ECL-Compatible Output Drivers in0.8 micron CMOS," *IEEE J. Solid-State Circuits*, vol. **30**, no. 12, pp.1463–1473, Dec. 1995.

[3] A. Bellaouar, M. S. O' Brecht, A. M. Fahim and M. I. Elmasry," Low power Direct Digital Frequency Synthesis for Wireless Communications," *IEEE J. Solid-State Circuits*, vol. **35**, no. 3, pp. 385–390, Mar. 2000.

[4] M. M. El Said and M. I. Elmasry, "An Improved ROM Compression Technique for Direct Digital Frequency Synthesizers," in *Proc. IEEES ymp. Circuits and Systems Paper*, vol. **5**, May 2002, pp. 437–440.

[5] W. Lee and I. C. Park, "Quadrature Direct Digital Frequency Synthesis Using Fine-Grain Angle Rotation Technique," Electron. Lett, vol. **39**, no. 17, pp. 1235–1237, Aug. 2003.

[6] W.Akram, Jr. E.E Swartzlander, "Direct Digital Frequency Synthesis Using Piece-wise Polynomial Approximation," *IEEE Int. Signals, Systems and Computers Conf. Paper*, Vol. **2**, Nov. 2003, pp.2237 2241.

[7] B. D. Yang, J. H. Choi, S. H. Han, L. S. Kim and H. K. Yu, "An 800-MHz Low-Power Direct Digital Frequency Synthesizer with an on-Chip D/A Converter," *IEEE J. Solid-State Circuits*, vol. **39**, no. 5, pp. 761–774, May 2004.

[8] H. Jafari, A. Ayatollahi and S. Mirzakuchaki, "A Low Power, High SFDR, ROM-Less Direct Digital Frequency Synthesizer," in IE*EE Int. Microelectronics Conf. Paper*, Dec. 2005, pp. 50–54.

[9] A. G. M. Strollo, D. De Caro and N. Petra, "A 630 MHz, 76 mW Direct Digital Frequency Synthesizer Using Enhanced ROM Compression Technique," *IEEE J. Solid-State Circuits*, Vol. **42**, No. 2, pp.350–360,Feb. 2007.

[10] B.D. Yang, L.S. Kim and H.K.Yu, "A High Speed Direct DigitalFrequency Synthesizer Using a Low Power Pipelined Parallel Accumulator," *IEEE J. Circuit and Systems*, pp. V-373–V-376, May2002.

[11] D. De Caro, E. Napoli, and A. G. M. Strollo "High Speed Direct Digital Frequency Synthesizers in 0.25µm CMOS," in *IEEE Custom Integrated Circuits Conf. Paper*, Oct. 2004, pp.163166.

[12] J. M. P. Langlois, and D. Al-Khalili, "A Low Power Direc Digital Frequency Synthesizers in 0.18-mµ CMOS," in *IEEE Custom Integrated Circuits Conf. Paper*, Sept. 2003, pp.283–286.